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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,963	03/23/2004	Steven C. Goss	TI-36791	2345

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EXAMINER	
POWERS, WILLIAM S	
ART UNIT	PAPER NUMBER
2134	

NOTIFICATION DATE	DELIVERY MODE
06/24/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/806,963	GOSS, STEVEN C.	
	Examiner	Art Unit	
	WILLIAM S. POWERS	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, pages 4-5, filed 3/24/2008, with respect to the rejection(s) of claim(s) 1, 8 and 15 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection to the claim limitations regarding the secure memory coupled to the key register has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of "Using a High-Performance, Programmable Secure Coprocessor" by Smith et al.

2. As to Applicant's argument that Takahashi does not teach, "a cryptographic block coupled to a key register and data input and output registers," (Remarks, page 5, lines the Examiner respectfully disagrees. While Takahashi does not use the terminology "data input and output registers", Takahashi does use SRAM 18 for the storage of encrypted and decrypted instructions inputted and outputted to external memory (Takahashi, col. 3, liens 6-35). The Examiner equates the SRAM 18 of the secure memory management unit as equivalent to the input and output registers of the claim limitations. For at least the reasons above, the rejection of the abovementioned limitations is maintained.

Response to Amendment

3. The Examiner has stated the below column and line numbers as examples. All columns and line numbers in the reference and the figures are relevant material and Applicant should be taken the entire reference into consideration upon the reply to this Office Action.

4. Claims 1-20 are pending.

Information Disclosure Statement

5. No Information Disclosure Statement has been submitted by the Applicant.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,825,878 to Takahashi et al. (hereinafter Takahashi) in view of "Using a High-Performance, Programmable Secure Coprocessor" by Smith et al. (hereinafter Smith).

As to claims 1 and 8, Takahashi teaches:

a. A key register located within said SEE (key register with cryptographic keys stored within the key register) (Takahashi, column 5, lines 34-50 and figure 2).

Takahashi does not expressly mention a secure memory coupled to the key register. However, in an analogous art, Smith teaches said secure memory coupled to the key register to receive a cryptographic key therefrom (secure memory a private key used for authentication and decryption purposes) (Smith, page 77, lines 3-11).

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to implement the secure memory management unit of Takahashi with the secure memory of Smith in order to secure on-device applications as suggested by Smith (Smith, page 77, lines 3-11).

Takahashi as modified further teaches:

b. Data input and output registers located outside of said SEE and coupled to said key register to allow said cryptographic key to be applied to input data

arriving via said data input register to yield output data via said data output register (input and output is controlled by the memory controller that accesses the external memory and stores the input/output in SRAM) (Takahashi, Abstract, figure 1, column 3, lines 6-20 and column 6, lines 14-35).

As to claims 2, 9 and 16, Takahashi as modified teaches a secure data bus coupling said key register and said secure memory is isolated from external pins of said SoC (the integrated chip is constructed to prevent access to the internal buses and connectors of the chip) (Takahashi, column 2, lines 40-48 and figure 1).

As to claims 3, 10 and 17, Takahashi as modified teaches a cryptographic block coupled to said key register and said data input and output registers consists of a Data Encryption Standard (DES) block (uses the DES algorithm) (Takahashi, column 5, lines 16-22).

As to claim 4, 11 and 18, Takahashi as modified teaches said key register is a write-only register and writeable only when a central processing unit of said SoC is in a secure state (write request must be initiated by the internal OS) (Takahashi, column 6, lines 14-35).

As to claims 5, 12 and 19, Takahashi teaches as modified a data bus coupled to said input and output registers is further coupled to external pins of said SoC (memory

controller of the integrated chip is connected to the external memory, which is the only access to elements not on the chip) (Takahashi, column 6, lines 14-35 and figure 1).

As to claims 6, 13 and 20, Takahashi as modified teaches a central processing unit mediates movement of said input data and said output data between said input and output registers and memory external to said SoC (CPU core and DMA control the inputting, outputting, encryption and decryption of data) (Takahashi, column 4, lines 45-58 and figures 2 and 3).

As to claims 7 and 14, Takahashi as modified teaches said secure memory comprises secure read-only memory and secure static random access memory (integrated chip consists of SRAM and ROM that is located within the secure environment of the integrated chip) (Takahashi, figure 1, column 3, lines 6-20 and column 6, lines 43-47).

As to claim 15, Takahashi teaches:

a. A central processing unit (CPU) (Takahashi, column 2, lines 49-53 and figure 1).

b. Secure read only memory (integrated chip consists ROM that is located within the secure environment of the integrated chip) (Takahashi, column 6, lines 43-47).

c. Secure static random access memory, said CPU and said secure memory configured to provide a secure execution environment (integrated chip consists of SRAM that is located within the secure environment of the integrated chip) (Takahashi, figure 1, column 3, lines 6-20).

d. A key register located within said SEE (key register with cryptographic keys stored within the key register) (Takahashi, column 5, lines 34-50 and figure 2).

Takahashi does not expressly mention a secure memory coupled to the key register. However, in an analogous art, Smith teaches said secure memory coupled to the key register to receive a cryptographic key therefrom (secure memory a private key used for authentication and decryption purposes) (Smith, page 77, lines 3-11).

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to implement the secure memory management unit of Takahashi with the secure memory of Smith in order to secure on-device applications as suggested by Smith (Smith, page 77, lines 3-11).

Takahashi as modified further teaches:

e. Data input and output registers located outside of said SEE and coupled to said key register to allow said cryptographic key to be applied to input data arriving via said data input register to yield output data via said data output register (input and output is controlled by the memory controller the accesses the external memory and stores the input/output in SRAM) (Takahashi, Abstract, figure 1, column 3, lines 6-20 and column 6, lines 14-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM S. POWERS whose telephone number is (571)272-8573. The examiner can normally be reached on m-f 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 571 272 3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. S. P./
Examiner, Art Unit 2134

William S. Powers
Examiner
Art Unit 2134

6/17/2008

/Kambiz Zand/
Supervisory Patent Examiner, Art Unit 2134